CMOS , 140 MHz 10-Bit Triple High Speed DAC

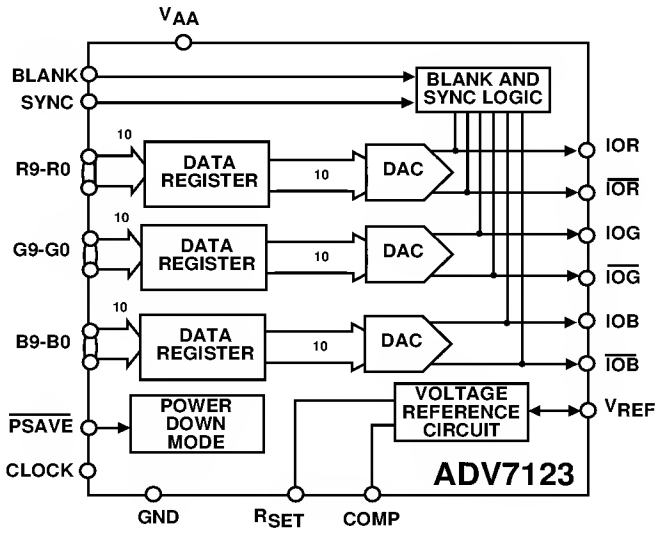
Preliminary Information

ADV7123

FEATURES
140 MSPS Throughput Rate
Triple 10-Bit D/A Converters
-48dB SFDR
RS-343A/RS-170 Compatible Output
Complimentary Outputs
TTL Compatible Inputs
Internal Reference
+5 V CMOS Monolithic Construction
48-Pin TQFP Package
Low Power Dissipation
Low Power Standby Mode
Industrial Temperature Range (-40°C - 85°C)

APPLICATIONS
Digital Video Systems
High Resolution Color Graphics
Digital Radio Modulation
Image Processing
Instrumentation
Video Signal Reconstruction

FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

The ADV7123* is a triple high speed, digital-to-analog converter on a single monolithic chip. It consists of a three high speed, 10-Bit, video D/A converters with complimentary outputs, a standard TTL input interface and a high impedance, analog output, current sources.

The ADV7123 has three separate 10-Bit wide input ports. A single +5V power supply, an optional external 1.235 V reference and clock are all that are required to make the part functional. The ADV7123 has additional video control signals, composite $\overline{\text{SYNC}}$ and $\overline{\text{BLANK}}$.
The ADV7123 also has a power down mode.

The ADV7123 is fabricated in a +5V CMOS process. Its monolithic CMOS construction ensures greater functionality with lower power dissipation. The ADV7123 is available in a 48-lead TQFP package.

PRODUCT HIGHLIGHTS

1.140 MSPS Throughput.

2. Guaranteed monotonic to 10 bits.

3. Compatible with a wide variety of high resolution color graphics systems including RS-343A and RS170A.

Prelim REV 1.0 AUG '96

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ADV7123–SPECIFICATIONS

(V_{AA}[1] = +5 V; V_{REF} = +1.235 V (ext); R_{SET} = 560 Ω, R_L = 37.5 Ω, C_L = 10 pF). All specifications T_{MIN} to T_{MAX}[2] unless otherwise noted.)

Parameter	V_{AA} = 3.3V[3]	Units	V_{AA} = 5V	Units	Test Conditions/Comments
STATIC PERFORMANCE					
Resolution (Each DAC)	10	Bits	10	Bits	
Accuracy (Each DAC)					
Integral Nonlinearity[3]	±1	LSB max	±1	LSB max	
Differential Nonlinearity[3]	±1	LSB max	±1	LSB max	Guaranteed Monotonic
Gray Scale Error	±5	% Gray Scale	±5	% Gray Scale	
Coding		Binary		Binary	
DIGITAL INPUTS					
Input High Voltage, V_{INH}	2.1	V min	2.4	V min	
Input Low Voltage, V_{INL}	0.6	V max	0.8	V max	
Input Current, I_{IN}	±1	µA max	±1	µA max	V_{IN} = 0.4 V or 2.4 V
Input Capacitance, C_{IN}	10	pF typ	10	pF typ	
ANALOG OUTPUT					
Current Range	tbd	mA min	15	mA min	
	tbd	mA max	22	mA max	
Output Current					
White Level	tbd	mA min	16.74	mA min	
		mA max	18.50	mA max	
Black Level	tbd	µA min	0	µA min	
	tbd	µA max	50	µA max	
LSB Size	tbd	µA typ	17.28	µA typ	
Output Compliance, V_{OC}	0	V min	0	V min	
	tbd	V max	+1.4	V max	
Output Impedance, R_{OUT}	100	kΩ typ	100	kΩ typ	
Output Capacitance, C_{OUT}	30	pF max	30	pF max	I_{OUT} = 0 mA
DYNAMIC PERFORMANCE					
SFDR[3,4]	-48	dBc max	-48	dBc max	FCLK = 125 MHz, FOUT = 2 MHz
SFDR[3,4]	-48	dBc max	-48	dBc max	FCLK = 100 MHz, FOUT = 2 MHz
SFDR[3,4]	-48	dBc max	-48	dBc max	FCLK = 125 MHz, FOUT = 16 MHz
SFDR[3,4]	-48	dBc max	-48	dBc max	FCLK = 100 MHz, FOUT = 16 MHz
SFDR[3,4]	-48	dBc max	-48	dBc max	FCLK = 125 MHz, FOUT = 40 MHz
SFDR[3,4]	-48	dBc max	-48	dBc max	FCLK = 100 MHz, FOUT = 40 MHz
Glitch Impulse	50	pV secs typ	50	pV secs typ	
DAC Noise[5]	200	pV secs typ	200	pV secs typ	
VOLTAGE REFERENCE					
Voltage Reference Range, V_{REF}	1.21	V min	1.21	V min	V_{REF} = 1.235 V (ext)
	1.235	V typ	1.235	V typ	
	1.26	V max	1.26	V max	
Input Current, I_{VREF}	10	mA typ	10	mA typ	
VOLTAGE REFERENCE (INT)[3]					
Voltage Reference Range, V_{REF}	1.21	V min	1.21	V min	
	1.235	V typ	1.235	V typ	
	1.26	V max	1.26	V max	
Output Impedance, R_{OUT}	100	kΩ typ	100	kΩ typ	
POWER REQUIREMENTS					
V_{AA}	3.3	V typ	5	V typ	
Digital Supply Current[6]	30	mA max	30	mA max	50 MHz
	30	mA max	30	mA max	140 MHz
Analog Supply Current[6]	tbd	mA max	tbd	mA max	
Standby Current	tbd	mA max	5	mA max	
Power Supply Rejection Ratio	0.5	%/% max	0.5	%/% max	COMP = 0.1 µF

NOTES

[1]±5% for all versions.

[2]Temperature range (T_{MIN} to T_{MAX}): -40°C to +85°C. Max Junction Temperature T_J=110°C

[3]Guaranteed by Characterisation

[4]See Appendix A for performance Graphs: SFDR to Nyquist Frequency Plot, SFDR to -2 MHz Frequency window, SNR vs O/P Frequency plot and THD vs O/P Frequency plot.

[5]This includes effects due to clock and data feedthrough.

[6]Pixel port is continuously clocked with data corresponding to a linear ramp.

Specifications subject to change without notice.

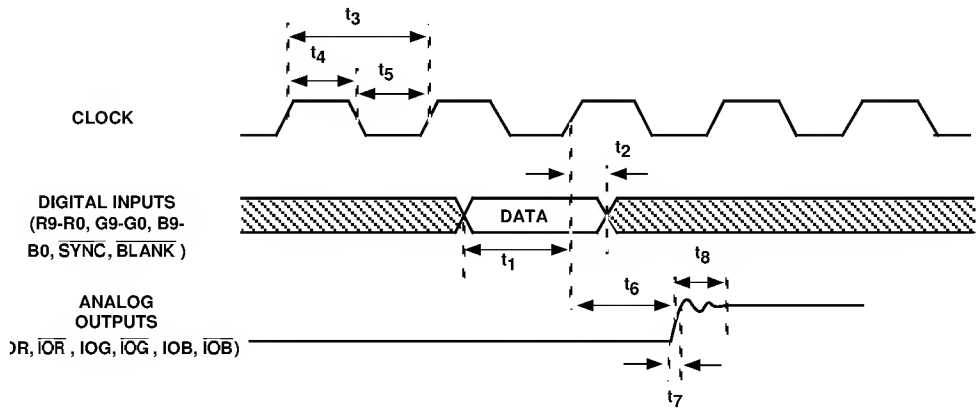
TIMING CHARACTERISTICS[1]

(V_{AA}= +5 V ±5%; V_{REF} = +1.235 V; R_L = 37.5 Ω, C_L = 10 pF; R_{SET} = 560 Ohms. All Specifications T_{min} to T_{max}[2] unless otherwise noted).

Parameter	140MHz Version	Units	Conditions/Comments
f_{max}	140	MHz max	Clock Rate
t_1[4]	2	ns min	Data & Control Setup Time
t_2[4]	2	ns min	Data & Control Hold Time
t_3[4]	7.1	ns min	Clock Cycle Time
t_4[4]	2.85	ns min	Clock Pulse Width High Time
t_5[4]	2.85	ns min	Clock Pulse Width Low Time
t_6	12	ns typ	Analog Output Delay
t_7	1	ns typ	Analog Output Rise/Fall Time
t_8[3]	12	ns typ	Analog Output Transition Time
t_{pline}	1	pclk	Pipeline Delay
t_{pdown}	tba	ns typ	Powerdown/Powerup Time

NOTES
[1]TTL input values are 0 to 3 volts, with input rise/fall times ≤3ns, measured between the 10% and 90% points. Timing reference points at 50% for inputs and outputs. See timing notes in Figure 1.
[2]Temperature Range (T_{min} to T_{max}); -40 to +85°C
[3]Sample Tested at 25°C to ensure compliance
[4]Guaranteed by Characterisation
Specifications subject to change without notice.

TIMING DIAGRAM



NOTES
1. Output delay (t_6) measured from the 50% point of the rising edge of CLOCK to the 50% point of full scale transition.
2. Output rise/fall time (t_7) measured between the 10% and 90% points of full scale transition.
3. Transition time (t_8) measured from the 50% point of full scale transition to within 2% of the final output value.

ORDERING INFORMATION[1]

Package	Speed 50MHz	Option 140 MHz
PlasticTQFP[2] (ST-48)	ADV7123KST50	ADV7123KST140

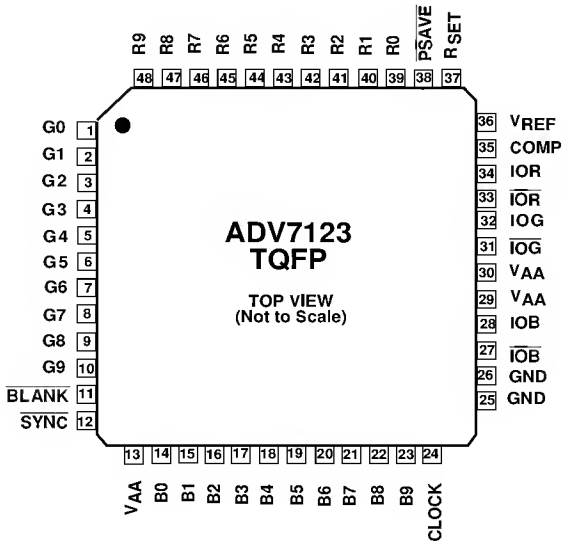
NOTES
[1] All devices are specified for -40 to +85°C operation
[2] TQFP Package

ABSOLUTE MAXIMUM RATINGS*

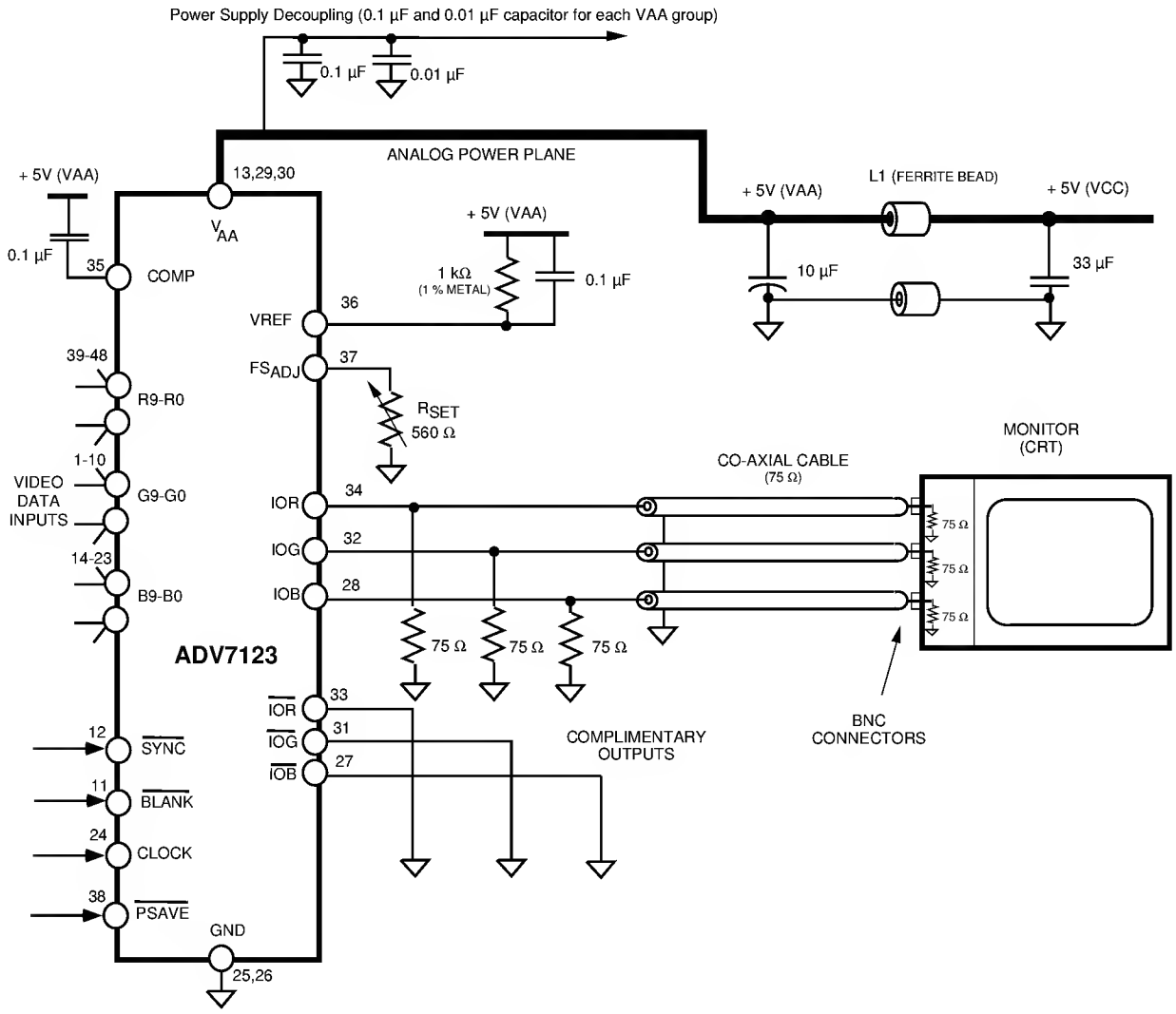
V_{AA} to GND.....+7V
Voltage on any Digital Pin.....GND-0.5V to V_{AA}+0.5V
Ambient Operating Temperature (T_A).....-40°C to +85°C
Storage Temperature (T_S).....-65°C to +150°C
Junction Temperature (T_J).....+150°C
Lead Temperature (Soldering, 10 secs).....300°C
Vapor Phase Soldering (1 minute)).....220°C
I_{OUT} to GND[1].....0V to V_{AA}

NOTES
*Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.
[1]Analog Output Short Circuit to any Power Supply or Common can be of an indefinite duration.

PIN CONFIGURATION
48 PIN TQFP



CAUTION
ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although the ADV7123 features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.



ADV7123 TYPICAL CONNECTION DIAGRAM

TABLE 1. VIDEO OUTPUT TRUTH TABLE (RSET = 560Ω, RLOAD = 37.5Ω

Description	IOG(mA)	$\overline{IOG}$ (mA)	IOR/IOB	$\overline{IOR}/\overline{IOB}$	$\overline{SYNC}$	$\overline{BLANK}$	DAC Input Data
WHITE LEVEL	25.24	0	17.62	0	1	1	3FFH
VIDEO	Video + 7.62	17.62 - Video	Video	17.62 - Video	1	1	Data
VIDEO to BLANK	Video	17.62 - Video	Video	17.62 - Video	0	1	Data
BLACK LEVEL	7.62	17.62	0	17.62	1	1	000H
BLACK to BLANK	0	17.62	0	17.62	0	1	000H
$\overline{BLANK}$ LEVEL	7.62	17.62	0	17.62	1	0	xxxH
$\overline{SYNC}$ LEVEL	0	17.62	0	17.62	0	0	xxxH

PACKAGE DIMENSIONS
48 PIN TQFP